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EXAMINER	
SINGH, DALIP K	
ART UNIT	**PAPER NUMBER**
2628	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/076,685	CHAMPION ET AL.	
	Examiner	Art Unit	
	Dalip K. Singh	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/22/06;9/12/05;6/*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's amendment dated June 13, 2005 ,in response to PTO Office Action dated March 10, 2005. Applicant's arguments filed July 29, 2002 have been fully considered but they are not persuasive.

2. Regarding applicant's argument with respect to claim 1 that, "portions of Takasugi disclose serial access to image data, but not the parallel storing and retrieving required by claim 1", Examiner disagrees. Takasugi reference (US 6,301,649 B1) **discloses** an input/output circuit E having an I/O terminal being electrically connected to the data bus pairs so as to perform a common input/output operation between the band-0 and the bank-1 (col. 9, lines 60-64). This is in fact is a classic example of parallel storing and retrieval of data from two memory banks.

3. With regards to applicant's argument for combining Reynolds-Takasugi references with Shreesha reference, Reynolds-Takasugi combination provides for faster access in row or column directions which then reduces data transfer latency from memory. Reynolds-Takasugi combination is lacking wherein the data elements stored are in consecutive order. Shreesha reference deals with image transposition memories where a video image needs to be filtered in both the vertical and horizontal directions (see background, col. 1, lines 11-15); and discloses a memory architecture is for a transpose memory employing SDRAM memory devices (col. 2, lines 9-11). Therefore, Shreesha reference provides for improving memory operations and its use with Reynolds-Takasugi is proper.

4. With regards to applicant's argument for combining Emmot reference to modify Reynolds-Takasugi-Shreehsa-Jones combination, Emmot provides for optimized access when rendering two-dimensional area (col. 2, lines 59-65) which improves memory access thus improving rendering performance.

5. Regarding applicant's argument with respect to claims 5 and 62, 64-67 that, "Jones reference was not discussed in the office action", Examiner disagrees. Jones was cited on page 5 of Office Action dated March 10, 2005 wherein Jones et al. **discloses** two dimensional image being organized in a two dimensional gril pattern of cell, each cell containing a matrix of pixels (col. 2, lines 3-16). Further, applicant's argument that no reference has been made of any relationship between claim 5 and claims 62, 64-67, Examiner would like to point out that claim 5 and claims 62, 64-67 were rejected under different references and such rejections are made separately (please see paragraph 7 for claim 5 rejection and see paragraph 8 for claims 62, 64-67).

6. Regarding applicant's argument with respect to claims 62, 64-67, the use of Ahuja reference being not discussed in the office action, Examiner meant to introduce it as prior art made of record but not relied upon but inadvertently put in the rejections. This reference is thus not part of claim rejections.

7. The indicated allowability of claims 26, 56 and 57 are withdrawn in view of the newly discovered reference(s) to US 6,259,459 B1 to Middleton. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-4, 14, 42-44, 46, 47, 49-52, 54, and 58-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,150,679 to Reynolds in view of U.S. Patent No. 6,301,649 B1 to Takasugi, and further in view of U.S. Patent No. 6,496,192 B1 to Shreesha et al,

and in view of Applicant admitted prior art (Specification of the instant application and drawings).

a. Regarding claim 1, Reynolds **discloses** a data source (object receiver 51); a data destination (object builder 55); at least two memory devices (RAM 45, RAM 46)(Fig. 3). Reynolds **is silent about** a first order and a second order of providing and receiving data elements; data elements storage and retrieval in parallel from the memory devices. Takasugi **discloses** data elements storage and retrieval in parallel from the memory devices and **further discloses** a first order and second order of data elements processing and storage/retrieval in that high speed serial access in row and column direction is possible as well storage of data elements in multiple locations (...a memory comprised of a plurality of banks interleaving...different rows...high-speed...access in the column direction...by the memory...col. 4, lines 30-47; col. 5,lines 1-32). Takasugi reference (US 6,301,649 B1) further **discloses** an input/output circuit E having an I/O terminal being electrically connected to the data bus pairs so as to perform a common input/output operation between the band-0 and the bank-1 (col. 9, lines 60-64). This is in fact is a classic example of parallel storing and retrieval of data from two memory banks. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made of modify the device as taught by Reynolds with the feature "high speed serial access in row and column direction using memory banks for storage and retrieval of data elements" as taught by Takasugi **because** it provides for quick access in row or column directions thus reducing data transfer latency. However, Reynolds-Takasugi combination **fails to disclose** storing data elements that are consecutive. Shreesha et al. **discloses** storing adjacent pixel elements (col. 4, lines 17-65). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Reynolds-Takasugi combination with the feature

"storing adjacent pixel elements along one dimension of the image" as taught by Shreeesha et al. **because** it allows blocks of image data to be fetched without latency.

b. Regarding claim 2, Reynolds **discloses** video source (object receiver 51) providing pixel data to a memory controller (memory controllers 41 and 42); generation a source address in the memory controller (memory controllers 41 and 42)(...the tile builder...maps...into tile row and column addresses corresponding to locations in the RAM 45 and 46...col. 5, lines 8-26) providing the pixel data to the memory system (memory elements 45 and 46) and storing the pixel data to the memory system.

c. Regarding claim 3, Applicant admitted prior art (Specification, Fig. 4) **discloses** data switch arrangement that controls which memory device gets to store which data element.

d. Regarding claims 4 and 42, Reynolds discloses RAM memory elements 45 and 46 comprising an image buffer storage area (col. 5, lines 45-54).

e. Regarding claim 43, Takasugi discloses alternate memory accesses (...a memory comprised of a plurality of banks interleaving...different rows...high-speed...access in the column direction...by the memory...col. 4, lines 30-47; col. 5,lines 1-32).

f. Regarding claim 44, Takasugi implicitly discloses data elements are pixel data (col. 4, lines 30-47; col. 5,lines 1-32).

g. Regarding claim 46, Takasugi implicitly discloses burst accessing (...a memory comprised of a plurality of banks interleaving...different rows...high-speed...access in the column direction...by the memory...col. 4, lines 30-47; col. 5,lines 1-32).

h. Regarding claim 47, it is similar in scope to claim 1 above and is rejected under the same rationale.

i. Regarding claims 49 and 50, Takasugi implicitly discloses storage of pixels in two memory devices (col. 4, lines 30-47; col. 5,lines 1-32).

j. Regarding claim 51, it is similar in scope to claim 1 above and is rejected under the same rationale.

k. Regarding claim 52, Reynolds discloses data source being a video source (Fig. 3).

l. Regarding claim 54, Reynolds discloses data destination being a video display system (Fig. 2 & 3).

m. Regarding claims 58-61, it is similar in scope to claim 1 above and is rejected under the same rationale.

n. Regarding claim 14, it is similar in scope to claim 3 above and is rejected under the same rationale.

10. Claims 56 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,150,679 to Reynolds in view of U.S. Patent No. 6,301,649 B1 to Takasugi, and further in view of U.S. Patent No. 6,496,192 B1 to Shreesha et al, and in view of Applicant admitted prior art (Specification of the instant application and drawings), and further in view of US 6,259,459 B1 to Middleton.

a. Regarding claims 56 and 57, Reynolds-Takasugi-Shreesha-AAPA **does not disclose** data elements are pixel data for pixels in a frame, the first order being horizontal row order, and the second order being vertical column order; and wherein the first order is a vertical column order, and the second order is a horizontal row order. Middleton **disclose** data buffer memory 4 wherein the pixel data values can be read to perform image processing manipulations, such as horizontal, vertical or temporal filtering and the order in which the pixel data values need to be passed to the image processor 2 depends upon the manipulation being performed (col. 5, lines 49-57).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Reynolds-Takasugi-Shreesha-AAPA combination with the feature "image processing manipulations be it horizontal, vertical or temporal for pixel data values" as taught by Middleton **because** it allows for making full use of available bus bandwidth, and reducing burden on the image processor to provide reordering or bit slicing functions.

11. Claims 5, 6, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,150,679 to Reynolds in view of U.S. Patent No. 6,301,649 B1 to Takasugi, and further in view of U.S. Patent No. 6,496,192 B1 to Shreesha et al, and further Applicant admitted prior art (Specification of the instant application and drawings) as applied to claim 1 above and further in view of U.S. Patent No. 6,018,354 to Jones et al.

a. Regarding claim 5, Reynolds-Takasugi-Shreesha combination **does not disclose** correspondence between a data element being a pixel data in a frame of pixels, the frame having horizontal rows and vertical columns of pixels. Jones et al. **discloses** two dimensional image being organized in a two dimensional grid pattern of cells, each cell containing a matrix of pixels (col. 2, lines 3-16). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Reynolds-Takasugi-Shreesha combination with the feature "multi-dimensional relationship between pixels" as taught by Jones et al. **because** it improves data access when retrieving these words associated with a dimensional image.

b. Regarding claims 6 and 48, Reynolds **discloses** a memory controller (memory controllers 41 and 42).

12. Claims 7-13, 15-25, 27-41, 45, 53, 55 and 62-67 are rejected under 35 U.S.C. 103(a) are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,150,679 to Reynolds in view of U.S. Patent No. 6,301,649 B1 to Takasugi, and further in view of U.S. Patent

No. 6,496,192 B1 to Shreesha et al, and further Applicant admitted prior art (Specification of the instant application and drawings) as applied to claim 1 above and further in view of U.S. Patent No. 6,018,354 to Jones et al. and further in view of U.S. Patent No. 6,724,396 B1 to Emmot et al.

a. Regarding claims 7, Reynolds-Takasugi-Shreehsa-Jones combination is **silent about** memory controller having two states for storing data for a horizontal pixel pair, where a first pixel in the horizontal pixel pair is horizontally adjacent and to the left of a second pixel in the horizontal pixel pair; a first state where pixel data for the first pixel is stored in the first memory device and the second pixel is stored in the second memory device; and a second state where first pixel in the horizontal pixel pair is stored in the second memory device and the second pixel in the horizontal pixel pair is stored in the first memory device; and the same being true for vertical pixel pair with memory controller having two states wherein in the first state the first of the vertical pixel pair is stored in the first memory device and the adjacent second vertical pixel pair is stored in the second memory device and a second state where first of the vertical pixel pair is stored in the second memory device and second of the vertical pixel pair is stored in the first memory. Emmot et al. **discloses** such an arrangement (...allocation of texture maps 210....is stored in consecutive blocks...left area 212*l* is allocated to consecutive blocks...in second memory area 244...and right area 212*r* is allocated to...in first memory area...similarly right area 212*r* ...right area...is allocated to first memory area...right area 214*r* is allocated to second memory area 244...in an alternating patterns...the memory allocation...avoids consecutive accesses to different pages in the same bank...col. 8, lines 21-67; col. 9, lines 1-67; col. 10, 1-67). Although Emmot et al. discloses texture map allocation, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Reynolds-Takasugi-Shreehsa-Jones combination with the feature "allocation of image date in this case pixels data which are "correlated data sets"

among first and second memory areas" as taught by Emmot et al. **because** it reduces page miss penalty resulting in faster memory accesses.

b. Regarding claim 8, Reynolds-Takasugi-Shreehsa-Jones combination is **silent about** memory controller changing states. Emmot et al. **discloses** such an arrangement (...allocation of texture maps 210....is stored in consecutive blocks...left area 212*l* is allocated to consecutive blocks...in second memory area 244...and right area 212*r* is allocated to...in first memory area...similarly right area 212*r* ...right area...is allocated to first memory area...right area 214*r* is allocated to second memory area 244...in an alternating patterns...the memory allocation...avoids consecutive accesses to different pages in the same bank...col. 8, lines 21-67; col. 9, lines 1-67; col. 10, 1-67).

c. Regarding claims 9-13, Reynolds-Takasugi-Shreehsa-Jones combination is **silent about** memory controller having two states for storing data for a horizontal pixel pair, where a first pixel in the horizontal pixel pair is horizontally adjacent and to the left of a second pixel in the horizontal pixel pair; a first state where pixel data for the first pixel is stored in the first memory device and the second pixel is stored in the second memory device; and a second state where first pixel in the horizontal pixel pair is stored in the second memory device and the second pixel in the horizontal pixel pair is stored in the first memory device; and the same being true for vertical pixel pair with memory controller having two states wherein in the first state the first of the vertical pixel pair is stored in the first memory device and the adjacent second vertical pixel pair is stored in the second memory device and a second state where first of the vertical pixel pair is stored in the second memory device and second of the vertical pixel pair is stored in the first memory. Emmot et al. **discloses** such an arrangement (...allocation of texture maps 210...is stored in consecutive blocks...left area 212*l* is allocated to consecutive blocks...in second memory area 244...and right area 212*r* is allocated to...in first memory

area...similarly right area 212*r* ...right area...is allocated to first memory area...right area 214*r* is allocated to second memory area 244...in an alternating patterns...the memory allocation...avoids consecutive accesses to different pages in the same bank...col. 8, lines 21-67; col. 9, lines 1-67; col. 10, 1-67). Although Emmot et al. discloses texture map allocation, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Reynolds-Takasugi-Shreehsa-Jones combination with the feature "allocation of image date in this case pixels data which are "correlated data sets" among first and second memory areas" as taught by Emmot et al. **because** it reduces page miss penalty resulting in faster memory accesses.

d. Regarding claims 15 and 16, they are similar in scope to claims 12 and 13 and are rejected under the same rationale.

e. Regarding claim 17, it is similar in scope to claim 10 above and is rejected under the same rationale.

f. Regarding claims 18 and 19, Takasugi **discloses** data elements storage and retrieval in parallel from the memory devices and **further discloses** a first order and second order of data elements processing (col. 4, lines 30-47; col. 5, lines 1-32).

g. Regarding claims 20-22, Takasugi **discloses** data elements processing and storage/retrieval in that high speed serial access in row and column direction is possible as well storage of data elements ins multiple locations (...a memory comprised of a plurality of banks interleaving...different rows...high-speed...access in the column direction...by the memory...col. 4, lines 31-47; col.5, lines 1-32).

h. Regarding claims 23-25, Shreesha et al. **discloses** images containing 2048x 2048 pixel values and other image sizes such as 2048 x 1536, 2048 x 1024 et c. (col. 4, lines 65-67; table 1, col. 5). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to include 1920 x 1080 pixel as

well **because** it provides for flexibility from the point of view of end-user who might prefer different image sizes depending on the application that is in use.

i. Regarding claim 27, Reynolds-Takasugi-Shreehsa-Jones combination is **silent about** where pixel data for pixels in one pixel page is stored in a single page of memory. Emmot et al. **discloses** blocks of data representing each texture map in the series of texture maps being stored in consecutive blocks of memory (col. 4, lines 1-15). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Reynolds-Takasugi-Shreehsa-Jones combination with the feature "graphics data being stored in consecutive block of memory" as taught by Emmot et al. **because** it avoids memory page conflicts.

j. Regarding claims 28-31, Reynolds **implicitly discloses** the use of counter that may be used for keeping count of pixels, address generation (See Fig. 6, Row RD PTR 134, Main RD PTR 153).

k. Regarding claims 32-34, Shreesha et al. **implicitly discloses** different clock rates for different image sizes (col. 4, liens 65-67, table 1).

l. Regarding claims 35 and 55, Reynolds **discloses** a high performance graphics memory systems for graphics applications.

m. Regarding claims 36 and 53, they are similar in scope to claim 23 above and are rejected under the same rationale.

n. Regarding claims 37-41, Reynolds **discloses** a high performance graphics memory systems utilizing synchronous graphics random access memory using two-bank architecture, paging overhead being reduced as a result (col. 1, lines 15-65).

o. Regarding claim 45, it is similar in scope to claims 28-31 and is rejected under the same rationale.

p. Regarding claim 62-67, they are similar in scope to claims 7, 9, 10, 12, 13, 15 and 16 and are rejected under the same rationale.

13. Claim 26 is rejected under 35 U.S.C. 103(a) are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,150,679 to Reynolds in view of U.S. Patent No. 6,301,649 B1 to Takasugi, and further in view of U.S. Patent No. 6,496,192 B1 to Shreesha et al, and further Applicant admitted prior art (Specification of the instant application and drawings) as applied to claim 1 above and further in view of U.S. Patent No. 6,018,354 to Jones et al. and further in view of U.S. Patent No. 6,724,396 B1 to Emmot et al., and further in view of US 6,259,459 B1 to Middleton.

a. Regarding claim 26, Reynolds-Takasugi-Shreesha-AAPA-Jones-Emmot combination **does not disclose** pixel data for two adjacent pixels in the first order being stored in the same memory page as pixel data for two pixels adjacent in the second order. Middleton **discloses** data buffer memory that stores pixel data and allows for image processor to access these in different orders. In particular, the data may be written into the banks of memory cells in one order, but read from it in a different order. Also, Middleton **discloses** use of plurality of banks of memory for storing adjacent pixel data values in a direction perpendicular to said raster lines. (col. 2, lines 24-37; lines 51-60). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Reynolds-Takasugi-Shreesha-AAPA-Jones-Emmot combination with the feature "adjacent pixel data values in the first and second order being stored in the same memory page" as taught by Middleton **because** it provides for reducing processor burden of reordering or bit slicing functions.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Dalip K. Singh** whose telephone number is **(571) 272-7792**. The examiner can normally be reached on Mon-Friday (10:00AM-6: 30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Ulka Chauhan**, can be reached at **(571) 272-7782**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Please note that the new Central Official FAX number for application specific communications with the USPTO is **571-273-8300** (effective July 15, 2005).

Dalip K. Singh

Examiner, Art Unit 2628

dks

July 28, 2006

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER